IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re Application of:		PATENT APPLICATION		
Inventors:	Yoshi Ono, John F. Conley, Jr., and Pooran Chandra Joshi	Attornov Dooket No		
Serial No:	Not Yet Assigned	Attorney Docket No. SLA0830		
Filed:	Herewith			
Title:	CHARGE TRAP NON-VOLATILE MEMORY STRUCTURE FOR 2 BITS PER TRANSISTOR	; 		
	DECLARATION FOR PATENT	APPLICATION		
address and original, first (if plural nan	below named inventor, I hereby declare that citizenship are as stated below next to my and sole inventor (if one name is listed belones are listed below), of the subject matter waght on the invention entitled,	name; I believe that I am the ow), or the first and joint inventor		
CHARGE TRAP NON-VOLATILE MEMORY STRUCTURE FOR 2 BITS PER TRANSISTOR				
the specifica	ation of which (check applicable ones):			
X	is attached hereto;	•		
-	was filed with the above-identified "Filed" date and assigned the above-identified "Serial No.";			
_	was amended on (or amended through)	·		
I hereby state that I have reviewed and understand the contents of the above- identified specification, including the claims, as amended by any amendment(s) referred to above.				

§1.56.

I acknowledge the duty to disclose information, which is material to the examination of the application in accordance with Title 37, Code of Federal Regulations,

I hereby declare that all statements made herein of my own knowledge are true and that all statements made on information and belief are believed to be true, and further that these statements were made with the knowledge that willful false statements and the like so made are punishable by fine or imprisonment, or both, under Section 1001 of Title 18 of the United States Code and that such willful false statements may jeopardize the validity of the application or any patent issuing thereon.

Full name of sole or first inventor:	Yoshi Ono
Residence:	2526 NW 24th Circle Camas, WA98607
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Citizenship:	USA
Inventor's signature:	THEO
Date:	3/19/2004
******	********
•	
Full name of second inventor:	John F. Conley, Jr.
Residence:	4652 NW Walden St. Camas, WA 98607
Post Office Address:	Same
Citizenship:	/U.\$.A./
Inventor's signature:	Bh D M
Date: 3/19/04	

third inventor:	Pooran Chandra Joshi
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Citizenship:	India
Inventor's signature:	<u></u>
Date:	03/19/04

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In re Application of:

Yoshi Ono, John F. Conley, Jr., and

Pooran Chandra Joshi

Serial No:

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CHARGE TRAP NON-VOLATILE

MEMORY STRUCTURE FOR 2 BITS

PER TRANSISTOR

PATENT APPLICATION

Attorney Docket No. SLA0830

POWER OF ATTORNEY BY ASSIGNEE

Sharp Laboratories of America, Inc., a corporation of the State of Washington, Assignee of the entire right, title and interest in and to the above-identified patent application by an assignment document filed herewith, hereby appoints David C. Ripma, Reg. No. 27,672, Matthew D. Rabdau, Reg. No. 43,026, as its attorneys with full power of substitution and revocation, to prosecute this application and to transact all business in the Patent and Trademark Office connected therewith; said appointment to be to the exclusion of the inventor and the inventor's attorneys in accordance with the provisions of 37 C.F.R. §3.71.

Pursuant to 37 C.F.R. §3.73(b) the undersigned submits herewith the original of an assignment document from the inventor or inventors to Assignee, together with a cover sheet and the fee for recording same. The undersigned, whose title is supplied below, is authorized to sign this Power of Attorney on behalf of the Assignee.

Please direct all correspondence connected with this application to:

Date: March 19, 2004

David C. Ripma, Patent Counsel Sharp Laboratories of America, Inc. 5750 NW Pacific Rim Boulevard

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Telephone: (360) 834-8754 (360) 817-8505 Facsimile:

Assignee:

Sharp Laboratøries of America, Inc.

By:√ David C. Ripma

Patent Counse Title: